ZENMAT

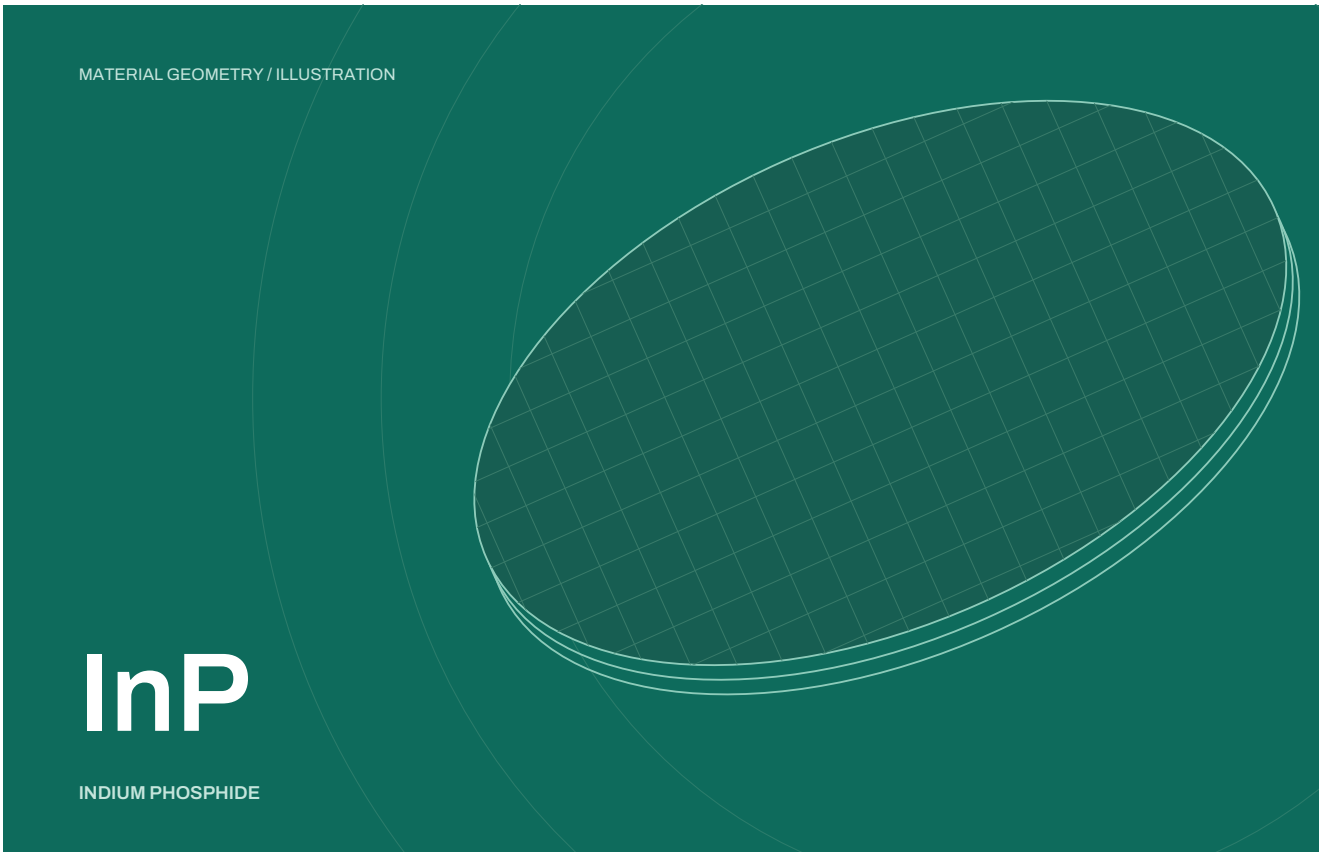
深圳臻材科技

PRODUCT GUIDE / EN

Indium phosphide substrates

Product guide

Clear specifications. Better conversations.



ZC-INP-PG-EN / V3.0

2026.09

Preliminary. Availability and warranted limits require written confirmation.

ABOUT ZENMAT

Start with material needs

ZENMAT focuses on indium phosphide single-crystal substrates and the material needs of optoelectronic and microelectronic applications. We believe material selection should begin with clear specifications, verifiable data and thorough technical discussion.

Make every material detail count.

This guide covers substrate selection, quality documentation and ordering. Specify diameter, conductivity type, dopant, surface finish and dislocation grade together. Suitability requires qualification in the customer's epitaxial and device process.

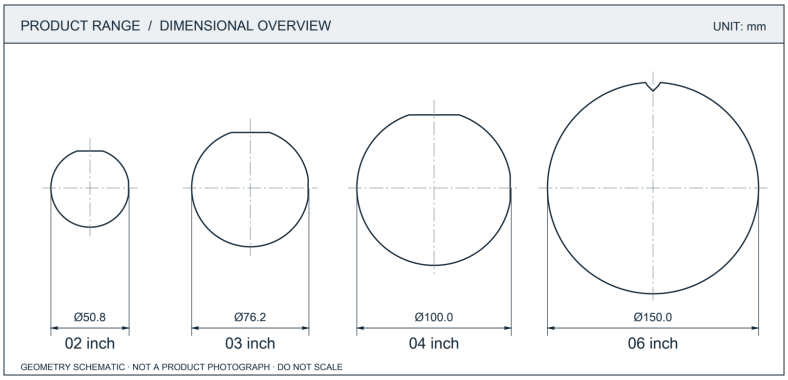
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Preliminary product guide. The values are requirements from GB/T 20230-2022, not a statement that all configurations are available. Availability, warranted limits and lead time are subject to the agreed written purchase specification. GB/T denotes a recommended Chinese national standard; these limits do not imply ISO or SEMI certification.

PRODUCT RANGE

Size range and alignment



Schematic of nominal size families and outlines; not a product photograph.

Nominal size	Diameter / mm	Thickness / µm	Alignment
2″	50.8±0.5	350±25	Primary / secondary flats
3″	76.2±0.5	600±25	Primary / secondary flats
4″	100.0±0.5	625±25	Primary / secondary flats
6″	150.0±0.5	675±25	Notch

Nominal inch sizes are product-family names. For 4- and 6-inch wafers, the specified diameters are 100.0 and 150.0 mm, not 101.6 and 152.4 mm. The 2-, 3- and 4-inch families use primary and secondary flats; the 6-inch family uses a notch.

Confirm the geometric interface

Include thickness and tolerances, orientation and tolerance, alignment features and surface finish in your enquiry. Detailed drawings and limits are provided in the accompanying technical specification and editable drawings.

Confirm availability for each combination of diameter, dopant, surface finish and dislocation grade. Supply configurations and volume-qualification status for 6-inch wafers remain subject to confirmation.

SPECIFICATION BASICS

Electrical and surface requirements

The electrical requirements below are retained from the previous technical materials. Electrical and dislocation results must be traceable to the corresponding ingot and linked to the lot and wafer identification.

Type / dopant	Resistivity Ω·cm	Carrier concentration cm^{-3}	Mobility $cm^2/(V·s)$
n / S	0.1×10^{-3}–6×10^{-3}	$\geq8\times10^{17}$	≥1,000
n / Sn	1×10^{-3}–6×10^{-3}	$\geq5\times10^{17}$	≥1,000
n / Undoped	—	$\leq1\times10^{16}$	≥3,500
p / Zn	—	$\geq5\times10^{17}$	≥50
SI / Fe	$\geq1\times10^{7}$	—	≥1,000

“—” means no value is specified, not zero. SI means semi-insulating.

Surface finish

P/E means a polished front surface and an etched back surface. P/P means both surfaces polished. Confirm the required finish and geometric limits against the downstream process.

Dislocation-density grades

Grade	I	II	III	IV	V
Limit / cm^{-2}	500	5,000	10,000	50,000	100,000

Availability by diameter, dopant and grade, and the supplier’s warranted limits, must be confirmed in the agreed purchase specification. See ZC-INP-TS-EN for full technical requirements.

QUALITY INFORMATION

Link records to the material

Quality records need to identify the material tested and the conditions of the test. Agree inspection items, methods, units and report formats during technical confirmation, and retain the relationship between ingot, lot and wafer.

Documentation	Traceability required
Ingot electrical and dislocation report	Ingot ID, wafer / lot ID, method, units and date
Wafer geometry, surface and particle inspection	Surface finish, inspection area, instrument and original results
Quality certificate and Certificate of Conformity (CoC)	Product designation, quantity, PO / lot reference and inspection authorization

From results to original records

Ingot electrical and dislocation results should reference the ingot ID. Wafer geometry, surface and particle results should reference the relevant lot or wafer. Agree how inspection area, instrument, date and original results will be documented.

Test images need context

Micrographs, inspection images and curves should state the sample identification, test conditions and any necessary calibrated scale. This guide does not display simulated micrographs or test curves. Quality decisions should rely on confirmed measured evidence.

This page describes documentation requirements and discussion points. It is not evidence of completed tests, certification or measured company performance.

HANDLING AND DELIVERY

Packaging and handling

Packaging

Under the existing technical materials, each wafer is individually packaged in a clean carrier, enclosed in clean plastic and aluminum-foil bags sealed under vacuum or nitrogen, then placed in a shipping carton. Confirm the actual packaging configuration in the order.

Incoming checks

Check package integrity, product labels and lot documents on receipt. Verify product identification, quantity and lot references. Retain packaging, labels and records if an issue is found, and follow the agreed handling procedure.

Transport and storage

Protect shipments from shock and moisture. Handle carefully and avoid dropping or crushing packages. Store in a clean, dry environment. Confirm temperature, humidity, shelf life and post-opening conditions separately.

Opening and wafer handling

Open in a process-appropriate clean environment. Handle the wafer at its edge with clean tools and avoid touching polished surfaces. Follow the supplier’s Safety Data Sheet (SDS) and site procedures for processing, cleaning and disposal.

Keep the package, label and report connected.

This guide does not replace the SDS, site procedures or the agreed acceptance specification. See the accompanying technical specification for detailed packaging and documentation requirements.

ORDERING INFORMATION

Order confirmation

Provide the information below when requesting a quotation. Confirm the available configuration, quantity, lead time and inspection scope in writing before issuing the purchase order.

RFQ item	Information to provide
Substrate configuration	Diameter, thickness and tolerances; conductivity type and dopant
Crystal and surface	Orientation and tolerance; flats or notch; P/E or P/P; dislocation grade
Inspection and documentation	Electrical limits, TTV, Warp, TIR, particle limits and required reports
Delivery information	Quantity, packaging, ship-to location, destination country and requested delivery date

GB/T Table 4 gives no TTV, Warp or TIR limits for 6-inch P/E wafers. Agree these separately if required.

Technical documents

Full technical requirements: ZC-INP-TS-EN, InP Technical Specification. The technical values are retained from the English materials dated 16 Sep 2026. This edition updates brand presentation and layout without adding company performance commitments.

Technical basis: GB/T 20230-2022, Indium phosphide single crystal. The technical specification, editable drawings and specification data workbook are included in the package.

Product enquiries

ZENMAT. Please provide the target size, conductivity type and dopant, surface finish, quantity and requested delivery date so that the technical requirements can be discussed in detail.

ZENMAT

Start with materials.
Plan the next step.

ZENMAT

Indium phosphide single-crystal substrates.
Product selection and technical discussion.

Clearer specifications. More precise communication.
Improvements supported by evidence.

Product configuration, inspection scope and delivery conditions are subject to written agreement.



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InP substrates